C-BAND HIGH POWER AND HIGH EFFICIENCY HARMONIC-TUNED OSCILLATOR

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ABSTRACT: In this paper, a high efficiency power oscillator is designed at C-band for the applications of wireless power transmission. A harmonic-tuning technique is adopted to achieve a high efficiency at a high frequency. It is also shown that the efficiency of the oscillator is degraded due to the reduced gain of the semi-conductor transistor at high frequency. The fabricated oscillator using GaN transistor shows an output power of 38.1 dBm with an efficiency of 58.4% at 5.71 GHz, which corresponds to the excellent performance among the reported oscillators around 5 GHz. © 2016 Wiley Periodicals, Inc. Microwave Opt Technol Lett 58:2281–2285, 2016; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.30025

Key words: efficiency; oscillator; power; wireless power transfer

1. INTRODUCTION

A solar power satellite (SPS) has been considered one of the promising candidates for a renewable energy system. It is based on long-range wireless power transmission utilizing microwave frequencies to effectively radiate and receive the electrical energy in the form of electromagnetic waves [1].

The oscillator, a DC-to-RF conversion circuit, is one of the key components of wireless communication and wireless power transmission systems. There have been extensive researches on high-frequency oscillators with high output power and high efficiency. Class-F and or class-E operation is a common approach to achieve high power and high efficiency performance [2,3]. However, the performance is highly limited by the switching loss as the frequency increases. The harmonic-tuned oscillator, on the contrary, is known to be able to exhibit better performance at higher frequency [4]. The authors of this paper have reported a harmonic-tuned power oscillator with high efficiency at 2.45 GHz for wireless power transfer such as the SPS [5].

Recently, the feasibility of the SPS system has been thoroughly investigated at a frequency as high as C-band (5.8 GHz) for the reduced circuit size and light weight [1]. However, the performance of the semi-conductor transistors is degraded as the frequency increases. For example, the gain and output power are inversely proportional to frequency squared, which limits output power and efficiency available from power amplifiers (PAs) and oscillators [1].

In this work, a high efficiency and high power oscillator is designed at 5.8 GHz using a non-linear design technique proposed in Ref. [5]. The performance degradation of the oscillator at higher frequency is also discussed in terms of output power and efficiency. The measurement of the oscillator using GaN high electron mobility transistor (HEMT) shows the high efficiency with high output power at C-band, which can be effectively applied to the wireless power transmission.

2. DESIGN OF HIGH-EFFICIENCY OSCILLATOR

In this work, the high-efficiency power oscillator is designed at 5.8 GHz using Cree GaN HEMT (CGH40006P) of which the performance was verified up to 6 GHz by the vendor. The bias is set to class AB, that is, a drain bias voltage of $V_{DD} = 28$ V and gate bias voltage of $V_{GG} = -2.8$ V. Figure 1 shows the block diagram of the designed oscillator, consisting of feedback network, output matching network (OMN), input matching network (IMN), and resonant circuits. The oscillator is designed according to the proposed non-linear design technique of the harmonic-tuned oscillator by the authors in Ref. [5]. At first, the optimum source and load impedances of the transistor presenting high-efficiency and high-power performance are determined at harmonic frequencies by the simulation. Then, the feedback network is synthesized at a fundamental frequency ($f_0 = 5.8$ GHz) allowing for the oscillation. Finally, the output and IMNs are designed at harmonic frequencies to present the optimum impedances.

2.1. Determination of Optimum Impedances

The optimum load and source impedances are determined for the transistor to provide high efficiency and high power by the load- and source-pull simulations with third harmonics considered. The determined optimum load and source impedances are as follows: $Z_{Lopt,1} = 10.1-j1.4$ Ω and $Z_{Sopt,1} = 11.8-j43$ Ω at $f_0$, $Z_{Lopt,2} = j164$ Ω and $Z_{Sopt,2} = j11.5$ Ω at $2f_0$, and $Z_{Lopt,3} = j133$ Ω and $Z_{Sopt,3} = j6.5$ Ω at $3f_0$, respectively. The large-signal simulation shows that the

Figure 1  Block diagram of the harmonic-tuned oscillator. Resonators have the same resonant frequency of $f_0$
PA with the drain and gate terminated with these optimum impedances exhibits the maximum power added efficiency (PAE) of 73.7% and maximum drain efficiency (DE) of 82.7% providing output power ($P_{\text{out}}$) of 39.1 dBm and power gain of 9.1 dB.

2.2. Design of Feedback Network
The feedback network in Figure 1 allows the closed loop gain to be greater than unity at $f_0$, leading to the oscillation. It should be designed to provide the optimum load and source impedances to the transistor at $f_0$. In Refs. 5, 6, it is shown that the feedback network can be synthesized from the voltages and currents at the gate and drain ($V_{\text{in}}, V_{\text{out}}, I_{\text{in}}$ and $I_{\text{out}}$ in Fig. 1), which are obtained from the load- and source-full simulations. By using the equations given in Refs. 5, 6, we determined a $\pi$-type feedback network consisting of reactive parts $B_1 = 8.91 \text{ mS}, B_2 = 5.99 \text{ mS}, B_3 = 17.98 \text{ mS}$ and real part $R_1 = 1/G_1 = 11.55 \Omega$, where the latter is implemented in the (OMN). The reactive parts are implemented by using the distributed elements instead of the capacitors to minimize the parasitic effect of chip components.

2.3. Design of OMN
The OMN is designed to provide $R_1$ at $f_0$, and $Z_{L,\text{opt},2}$ and $Z_{L,\text{opt},3}$ at $2f_0$ and $3f_0$, respectively. The series resonator at the drain side of the feedback network provides open-circuit at $2f_0$ and $3f_0$, so that the feedback network has no effect on load impedances at those frequencies. Therefore, the load network can be designed independently from the feedback network. Figure 2 shows the designed OMN using distributed elements, where open stubs and short transmission lines provide highly inductive impedance at $2f_0$ and $3f_0$.
2.4. Design of IMN

The IMN does not entangle the impedance at $f_0$, implemented by the feedback network due to the open-circuit performance at $f_0$ of the parallel resonator at the gate. Therefore, we only design the IMN to provide the optimum source impedances at $2f_0$ and $3f_0$. However, it is found from the simulation that the designed IMN at $2f_0$ and $3f_0$ marginally increases the efficiency by only 0.4%, so that the IMN and parallel resonators were omitted to reduce the associated loss and circuit size.

2.5. Suppression of Parasitic Oscillation

Large-signal loop-gain simulation was performed to verify the oscillation frequency. It showed that the designed oscillator was vulnerable to parasitic oscillations around 1 GHz. To remove these low-frequency parasitic oscillations, the edge-coupled line in Figure 3(a) was inserted in the feedback network [7]. It exhibits a band-pass filter performance as shown in Figure 3(b) with $S_{21}$ of $-12.4$ dB at 1 GHz while providing enough $S_{21}$ of $-3.5$ dB at $f_0 = 5.8$ GHz.

3. SIMULATION AND DISCUSSION

Figure 4 shows the final design of the oscillator. Note that the long transmission line is added in the feedback network to compensate for the added phase delay by the edge-coupled line.

Table 1 compares the simulated performance of the ideal PA, ideal oscillator, and practical oscillator, where “ideal” indicates the circuit consisting of ideal components without any parasitic effect and loss. In the first place, this table verifies that the oscillators were properly designed to provide the optimum harmonic load impedances determined by the load-full simulations.

With regard to the efficiency performance, the ideal oscillator exhibits DE of 73.7% which is much lower than DE (82.7%) but equal to PAE of the ideal PA. In addition, the ideal oscillator shows a reduced $P_{out}$ compared with the ideal PA. This observation can be explained by the power leakage to

Table 1 Simulation Result of PA and Oscillators

<table>
<thead>
<tr>
<th></th>
<th>$P_{out}$ (dBm)</th>
<th>DE (%)</th>
<th>$f_0$</th>
<th>$2f_0$</th>
<th>$3f_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal PA</td>
<td>39.1</td>
<td>82.7</td>
<td>10.1</td>
<td>-j1.4</td>
<td>j164</td>
</tr>
<tr>
<td>Ideal oscillator</td>
<td>38.6</td>
<td>73.7</td>
<td>10.2</td>
<td>j1.3</td>
<td>j165</td>
</tr>
<tr>
<td>Practical oscillator</td>
<td>38.2</td>
<td>65.1</td>
<td>10.8</td>
<td>j1.1</td>
<td>j166</td>
</tr>
</tbody>
</table>
the feedback network of the oscillator. In the oscillator, the generated power at the drain of the transistor \((P_{\text{drain}})\) is partly delivered to the feedback network \((P_{\text{feedback}})\) as indicated in Figure 4. That is, the delivered power to the load \((P_{\text{load}})\) is lower than \(P_{\text{drain}}\) by the amount of \(P_{\text{feedback}}\). The \(P_{\text{feedback}}\) finally is injected to the gate, which corresponds to input power in PA. In the designed oscillator, \(P_{\text{drain}} = 8.14\, \text{W}, P_{\text{feedback}} = 0.82\, \text{W}, \) and \(P_{\text{load}} = 7.32\, \text{W}.\) Therefore, \(P_{\text{out}}\) of the oscillator with feedback network is less than that of PA, reducing the efficiency. In other words, the efficiency of oscillator follows not DE but PAE of the PA.

By the way, PAE is generally lower than DE, because 
\[
\text{PAE} = \text{DE} \left( 1 - \frac{1}{G} \right),
\]
where \(G\) is a power gain. If \(G\) is high enough, \(\text{PAE} \cong \text{DE}.\) But PAE becomes lower than DE at low gain because of power dissipation at the gate of transistor. Unfortunately, the gain of solid-state transistors is inversely proportional to the frequency squared. It implies that PAE of the PA and the efficiency of the oscillator with the feedback network will be seriously degraded as the operating frequency increases. The GaN HEMT used in this work exhibits a gain of 9.1 dB at an oscillation frequency of 5.8 GHz, when it is terminated with optimum impedances. This low gain causes the efficiency of the ideal oscillator to be reduced, even though the transistor exhibits much higher DE.

The practical oscillator was fabricated in the microstrip lines on 20-mil-thick Taconic TLY-5 substrate with dielectric constant of 2.2. The capacitors were implemented using Murata chip elements (GJM1555C1H). The practical oscillator exhibits the simulated efficiency of 65.1% with \(P_{\text{out}}\) of 38.2 dBm. The efficiency is degraded by 6.1% compared with the ideal oscillator, which seems to be caused by the loss of chip components and long transmission lines in the feedback network.

4. EXPERIMENTAL RESULTS

Figure 5 shows the photograph of the fabricated oscillator which measures 48 mm \(\times\) 47 mm. The transistor was directly mounted on the aluminum jig for good heat sinking. Many screws were used to tightly contact the circuit board to the aluminum jig. The inductor in the series resonator was replaced with high-quality factor transmission line. The capacitors with value higher than 1 \(\mu\text{F}\) were used at the gate and drain bias lines to minimize the voltage fluctuations of the power supply.

The fabricated oscillator was measured at various bias conditions as shown in Figure 6. The \(P_{\text{out}}\) was measured by Agilent power meter (E4417A). Figure 6(a) shows the measured \(P_{\text{out}}\) and efficiency as a function of \(V_{\text{GG}}\) with a fixed \(V_{\text{DD}}\) of 28 V. The maximum efficiency of 58.4% is achieved at \(V_{\text{GG}} = -2.8\, \text{V}\), at which the output power is 38.1 dBm and the oscillation frequency is 5.71 GHz. Figure 6(b) shows the measured performance as a function of \(V_{\text{DD}}\) at a fixed \(V_{\text{GG}}\) of 
\[
-2.8\, \text{V}.
\]
The efficiency was maximized. No parasitic oscillation is observed and second harmonic component is suppressed by 36.09 dB compared with the fundamental one. The phase noise performance was also measured by using Anritsu spectrum analyzer (MS2830A). It was as good as 99.9 dB and 127.9 dBC/Hz at an offset frequency of 100 and 1000 kHz, respectively.

Table 2 compares the performance \((P_{\text{out}}, \text{efficiency})\) of the reported oscillator operating around 5.8 GHz [8-12]. Figure of merit \((\text{FoM})\) of the oscillator was also included [5,13]. The fabricated oscillator in this work shows an excellent efficiency performance with the highest \(P_{\text{out}}\) with comparable phase noise performance.

5. CONCLUSION

In this work, a high efficiency oscillator with high output power was designed at C-band using harmonic-tuning technique. It was shown that the efficiency of the oscillator could be degraded at a high oscillation frequency because of the reduced gain of the transistor. In order to improve the efficiency, the loss in the feedback network was minimized by using distributed elements replacing lumped elements. The fabricated oscillator exhibits an excellent performance in the efficiency and output power, so that it can be successfully applied to the high-power wireless power transmission over a long distance operating at C-band (5.8 GHz).

REFERENCES

ERRATUM FOR: SINGLE HALF-EFFECTIVE-WAVELENGTH-THICK DIELECTRIC LAYER

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In the above-mentioned article, which appeared in Microwave and Optical Technology Letters, Volume 58#7, DOI 29893, the title published was not the full title. The corrected, complete title is listed below:
HIGH-GAIN WIDEBAND RESONANT CAVITY ANTENNA WITH SINGLE HALF-EFFECTIVE–WAVELENGTH-THICK DIELECTRIC LAYER

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ERRATUM FOR: A WEARABLE ULTRA-WIDEBAND ANTENNA FOR WIRELESS BODY AREA NETWORKS

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In the above-mentioned article, which appeared in Microwave and Optical Technology Letters, Volume 58#7, DOI 29886, the first affiliation was not listed correctly. The correct affiliation is listed below:
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ERRATUM FOR: DESIGN OF A WIDEBAND DUAL-POLARIZED MICROSTRIP PATCH ANTENNA WITH NOVEL STRUCTURE FOR WLAN APPLICATION

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