A Broadband Power-Reconfigurable Distributed Amplifier

Jihoon Kim[1], Youngmin Kim[1], Sangho Lee[1], Jinho Jeong[2] and Youngwoo Kwon[1]

[1]Department of EECS and INMC, Seoul National University, Seoul, Korea
[2]Department of Electronic Engineering, Sogang University, Seoul, Korea

***ABSTRACT* — A broadband power-reconfigurable distributed amplifier (DA) is presented, where a triple-stack FET structure is employed as a power-adjustable gain cell. The output power is reconfigured by employing double gate-bias control scheme to the bottom and middle FET's, which maintains the efficiency under power back-off without degrading input and output return losses. The DA with eight gain cells is fabricated using a commercial 0.15 μm GaAs pHEMT process. In high power mode, the DA shows output power of 26.7 ~ 18.3 dBm from 1 to 40 GHz. In the low power mode, the output power is reconfigured to 25.2 ~ 14.2 dBm with the same input power. The efficiency degradation was less than 2 %. The control scheme can also be switched to analog mode to set continuous output power with minimal efficiency degradation.**

***Index Terms* — distributed amplifier, MMIC, pHEMT, power, reconfigurable, stacked FET**

I. INTRODUCTION

The development of modern communication systems have brought about many applications at various frequency bands. Recently, the area of wireless systems is rapidly expanding from microwave spectrum to quasi-millimeter or millimeter wave range [1] due to the need for broadband communications such as wireless high-definition multimedia interface (HDMI), streaming videos and high-speed internet access [2]. Various millimeter-wave frequency ranges have been allocated for military and commercial applications ranging from K-band through W-band. Instead of using dedicated narrow-band RF components for each band, it will be beneficial in terms of the cost and size of RF front-ends if microwave and millimeter-wave circuits are capable of the multi-band and multi-mode operations. In other words, reconfigurable RF-front ends are highly beneficial for this purpose.

A power amplifier (PA) is one of the core components that draws special attention in terms of reconfigurability. Since the efficiency of the PA drops drastically when the output power is backed off from the target output power, it is virtually impossible to maintain the PA efficiency for multi-mode operations requiring different target output power levels. Reconfigurable PA has recently been demonstrated to cover various output power levels and frequency bands with a single PA core for 2 GHz-band global roaming [3]. However, no power reconfigurable PA has been demonstrated at mm-wave frequencies.

This work presents a broadband power-reconfigurable PA, which can reconfigure the output power levels over ultra wide band frequencies. To cover a large bandwidth from a few GHz to millimeter-waves, a distributed amplifier (DA) is selected as an amplifier topology. The core unit cell of the DA is a triple-stacked FET, which works as a power-adjustable unit cell. Double gate-bias control scheme allows the amplifier to maintain the efficiency under power back-off conditions. Triple stack structure also provides the additional benefit of the increased output power compared with the conventional cascode cell [6][7], and helps to maintain the input and output return losses during reconfiguration. The eight-gain-cell DA fabricated with 0.15 μm GaAs pHEMT process reconfigures the output power from 18~27 dBm to 14~25 dBm between 1 and 40 GHz with minimal degradation in the efficiency. This work is among the first demonstrations of a broadband power-reconfigurable amplifier up to millimeter-waves.

II. POWER RECONFIGURABLE DESIGN

Figure 1 (a) shows the schematic of the proposed power reconfigurable DA with eight gain cells. The gain cell consists of triple-stacked FET as illustrated in Fig. 1 (b). The gate bias to each FET is applied through a large resistor such that each FET is biased to the same gate-source and drain-source voltages (V_{GG1} and $V_{DD}/3$) in the high power mode (HPM), where the DA is configured to operate at its maximum output power. The values of the gate capacitors C_{gg2} and C_{gg3} are carefully determined to optimize the output power (P_{out}) and the drain efficiency (DE). The triple-stacked FET tends to become unstable at high frequencies, as is often the case for the cascode FET. In order to prevent the instability over the entire bandwidth, two feedback resistors R_{GF1} and R_{GF2} are used at the gate terminals of M2 and M3 as shown in Fig. 1 (b). In particular, the value of R_{GF2} can be tuned after IC fabrication as it is realized with a variable resistor (controlled by V_{FC}). Drain termination load is also implemented with the variable resistor (controlled by V_{CONT}) to improve the return loss characteristics [4].

For operation in the low-power mode (LPM) when lower P_{out} by 3-4 dB is required, lower V_{GG2} is applied to the gate of middle FET (M2) which then pulls down the drain bias voltage of the bottom transistor (M1) in the triple-stack. This results in the early power saturation in M1 and reduces the output power from the stacked cell. In order to maintain the efficiency in LPM, the DC power consumption needs to be scaled back in the same ratio. Lowering V_{GG2} alone cannot achieve this goal since the overall DC voltage of the stacked-FET cell is fixed at V_{DD}. Additional DC current scaling is required to keep the overall efficiency constant in LPM. This

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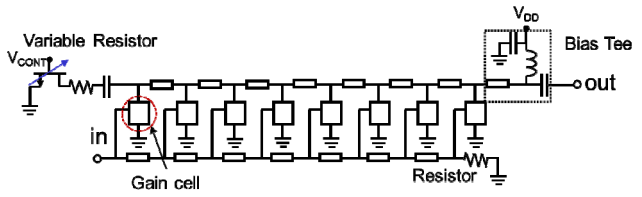
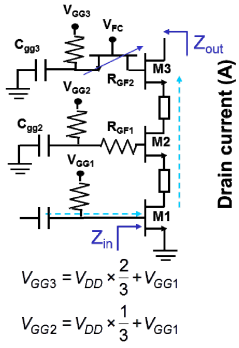


(a)



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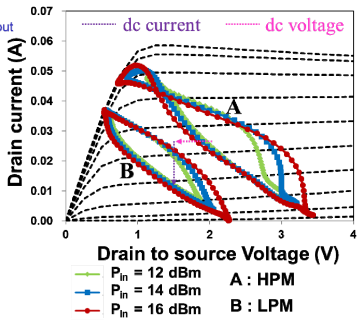


(c)

Fig.1. (a) Circuit schematic of the proposed DA (b) Triple-stacked FET structure of a gain cell. (c) Simulated load line of M1 depending on power modes at 10 GHz

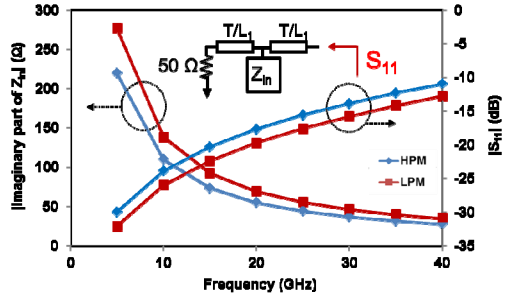


Fig.2. Calculated input impedance of a gain cell and return loss of a single gate-line section in HPM and LPM (T/L_1 is an ideal transmission line of 77 ∠6.8° at 20 GHz)

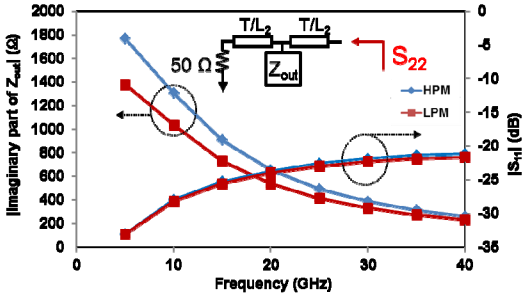


Fig.3. Calculated output impedance of a gain cell and return loss of a single drain-line section in HPM and LPM (T/L_2 is an ideal transmission line of 70 ∠8° at 20 GHz)

is achieved by lowering V_{GG1} at the same time, which reduces the DC current shared by all the transistors in the stacked cell. Fig. 1 (c) shows the calculated dynamic load line of M1 when V_{GG2} and V_{GG1} are lowered from 1.6V and -0.5V for HPM to 0.5V and -0.9V for LPM, respectively. It is clearly demonstrated that the output power of M1 is decreased by

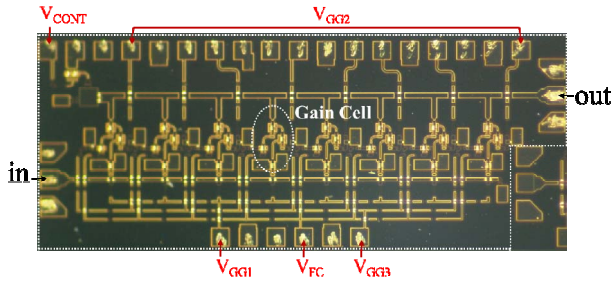
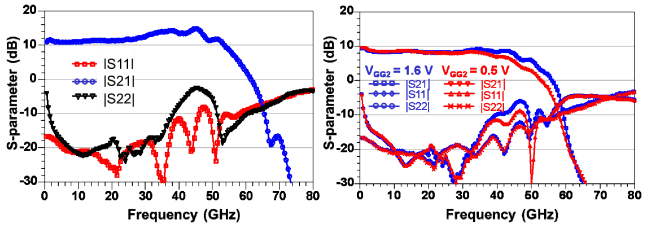


Fig. 4. Die photograph of the proposed DA



(a) (b)

Fig. 5. Measured S-parameter of the fabricated DA at V_{DD} = 6.4 V, V_{GG3} = 3.0 V, V_{CONT} = -1.0 V (a) HPM: V_{GG2} = 1.6 V, V_{GG1} = -0.5 V, V_{FC} = 1.97 V, (b) LPM: V_{GG2} = 0.5 ~ 1.6 V, V_{GG1} = -0.9 V, V_{FC} = 2.4 V

limiting the RF voltage and current swing. At the same time, the DC power consumption by M1 is also scaled back to maintain the efficiency in LPM.

Although we have changed V_{GG1} and V_{GG2} to control the output power and gain, it does not affect the input and output impedances (Z_{in}, Z_{out}) of the triple-stacked FET significantly [5]. Figure 2 and 3 shows the calculated Z_{in} and Z_{out} in HPM and LPM, and corresponding input and output return losses of the DA using a single gain cell as shown in the inset of the figures. Good impedance matching can be obtained in both LPM and HPM with the proposed method of double gate-bias control (V_{GG1} and V_{GG2}). It is worthwhile to note that the proposed method controls the gate bias only and thus does not require DC-DC converters for power reconfigurability.

Ⅲ. Measurement

A. *S-parameters measurement*

The proposed circuit has been fabricated using a commercial 0.15 μm GaAs pHEMT MMIC process with f_T of 85 GHz and f_{MAX} of 190 GHz. Fig. 4 shows the chip photograph. The chip size is 2.8 mm × 1.4 mm. Fig. 5 (a) shows the measured S-parameters of DA in HPM. V_{FC} and V_{CONT} are adjusted to prevent high-frequency oscillation. V_{GG3} is slightly tuned to 3.0 V from the pre-set value of 3.7V to suppress out-of-band oscillation (~80 GHz). V_{GG3} tuning has minimal impact on in-band gain and P_{out}. The DA shows power gains higher than 10 dB from DC to 53 GHz with a peak gain of 14.8 dB at 45 GHz. Input return loss is better than 10 dB from DC to 46 GHz and output return loss is better than 10 dB from 1.5 to 38 GHz. Fig. 5 (b) shows the measured S-parameters of the DA reconfigured to operate in LPM, where V_{GG2} is decreased

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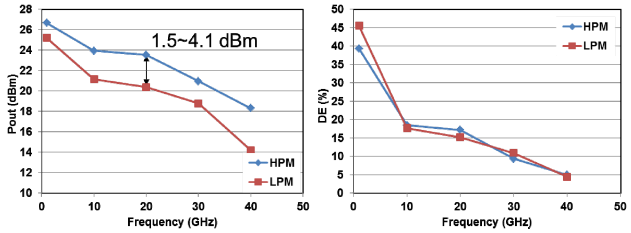
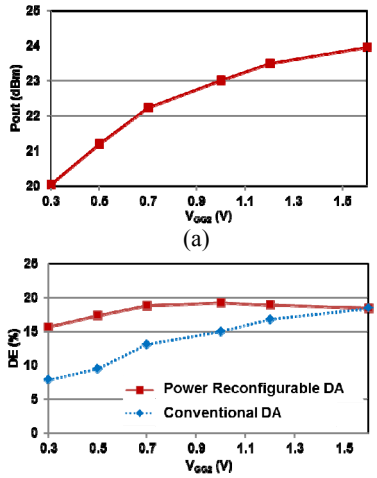


(a) (b)

Fig. 6. Measured (a) output power and (b) drain efficiency in HPM and LPM with the same input power



(a)

(b)

Fig. 7. Measured (a) P_{out} and (b) DE at 10 GHz as a function of V_{GG2}

from 1.6 to 0.5 V and V_{GG1} from -0.5 V to -0.9 V. As expected from the simulation, the DA maintains good input and output return losses in LPM. At $V_{GG2} = 0.5V$, gain is 6.0 ~ 9.4 dB from DC to 44 GHz. Input return loss is better than 10 dB from DC to 58 GHz and output return loss better than 10 dB from 1.5 GHz to 45 GHz. The measured data at $V_{GG2} = 1.6$ V are also inserted to show that V_{GG2} has minor effect on the gain and return losses in LPM.

B. power reconfigurable performance

In order to test the power reconfigurable characteristics of the proposed DA, the output power and drain efficiency are measured in both HPM and LPM. The results are compared at various frequencies (10, 20, 30, and 40 GHz) in Fig. 6. The same input power was used in both modes for comparison. In HPM, the DA delivers P_{out} of 26.7 ~ 18.3 dBm with the drain efficiencies of 39.3~4.9 % depending on the frequencies. In LPM, P_{out} is lowered by 1.5~4.1 dB compared to those in HPM while the efficiency remains virtually unchanged with less than 1.9 % degradation. Moreover, the output power of DA can be controlled in an analog fashion by controlling V_{GG2} and V_{GG1} continuously. Fig. 7 shows the measured P_{out} and DE as a function of V_{GG2} at 10 GHz. P_{out} is adjusted from 23.9 to 20.0 dBm while the drain efficiency varies from 18.5 to 15.7 %. Also shown in Fig. 7 (b) for comparison is the efficiency of a conventional DA under the similar power back off. Significantly higher efficiencies are achieved under power back-off using the proposed approach.

IV. Conclusion

A broadband power reconfigurable DA is demonstrated using a commercial 0.15 μm GaAs pHEMT technology. Distributed amplifier design results in broadband gain and matching performance. In addition, a triple-stacked FET structure together with double gate-bias control scheme (V_{GG1} and V_{GG2}) provides power reconfigurability over ultra wide band without degrading efficiency and return losses. It is also worthwhile to note that the proposed method does not require DC-DC converters for power reconfiguration. The proposed method can also be applied to the design of power-reconfigurable DA's using other technologies such as CMOS.

Acknowledgement

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