Broadband THz CMOS On-chip Antenna Using Stacked Resonators

Wonseok Choe and Jinho Jeong
Dept. of Electronic Engineering, Sogang University, Seoul, Korea
(choe0039@sogang.ac.kr, jjeong@sogang.ac.kr)

***Abstract*—In this paper, we present a broadband THz CMOS on-chip antenna. The bandwidth of the on-chip antenna is improved by stacking four resonators on the top of a standard patch antenna. The proposed antenna was fabricated using 65-nm CMOS process, and the performance was verified by simulation and measurement. The simulation and measurement results show that the antenna can exhibit the fractional bandwidth for 10-dB return loss greater than 10%, and radiation efficiency greater than 15% at 300 GHz.**

Keywords*—*THz; on-chip antenna; patch; resonator

I. Introduction

Recently, various THz monolithic integrated circuits (TMICs) have been reported in CMOS or InP HEMT technologies [1][2]. Besides the active circuits, THz antenna can also be integrated on-chip, which can reduce the production cost and minimize the performance degradation by the bonding wires which are needed to connect the active ICs and antenna.

However, most of the THz on-chip antennas have problems of low radiation efficiency and narrow bandwidth, which are caused by increased losses from substrate and conductors and very thin thickness of substrate between antenna and ground plane. Standard rectangular CMOS on-chip patch antennas have shown fractional bandwidth and radiation efficiency less than 10% [3].

This paper presents a broadband THz CMOS on-chip antenna with relatively high radiation efficiency. The antenna performances are improved by stacking four additional resonators on top of the patch antenna. The performance of the proposed antenna is verified by the simulation and measurement.

II. Design of The Proposed Antenna

A. Structure of the Proposed Antenna

Fig. 1 shows the structure of the proposed THz on-chip antenna. It is composed of feeding patch antenna and four top resonators. The four resonators on the same layer are stacked on top of the feeding patch antenna as shown in Fig. 1. They are coupled to the feeding patch, and are designed to have a different resonance frequency from a feeding patch. The multiple resonances of feeding patch and stacked resonators lead to the enhancement of bandwidth and radiation efficiency. The proposed antenna can be optimized by adjusting size of the stacked resonators (W_{SR}, L_{SR}) and feeding patch (W_F, L_F) and the spacing between the stacked resonators (G_{SR}). The dielectric constant and thickness of the substrate is 4.3 and 4.5 μm,

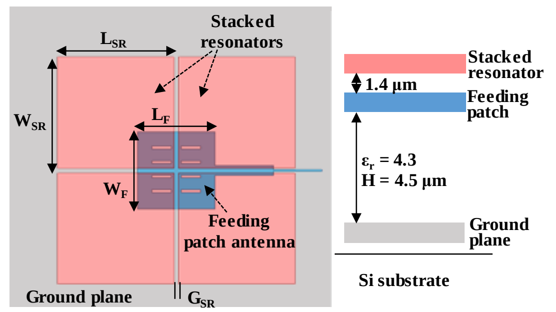

Fig. 1. Structure of the proposed THz CMOS on-chip antenna.

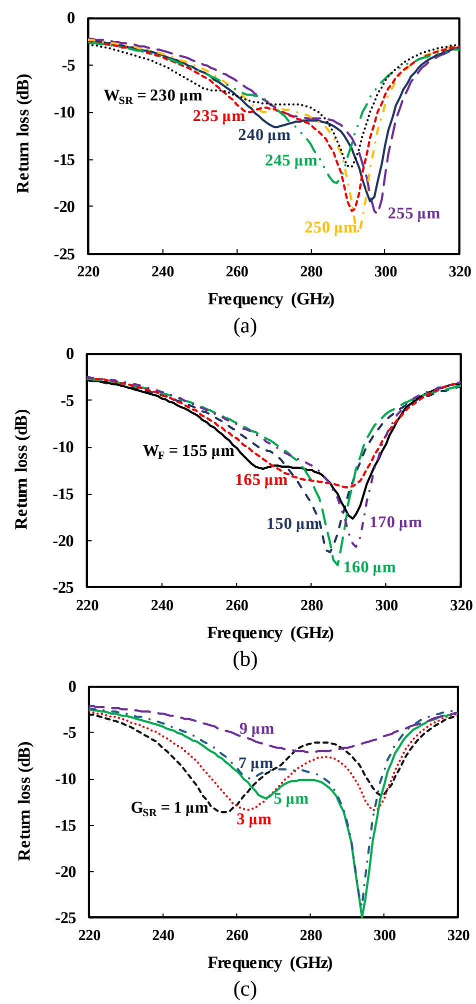

Fig. 2. Simulated return loss of the proposed antenna according to (a) W_{SR}, (b) W_F, and (c) G_{SR}.

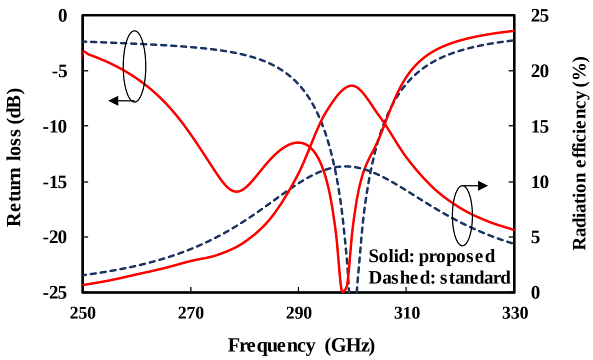

Fig. 3. Simulation results of the antennas (solid: the proposed antenna, dashed: standard rectangular patch antenna).

respectively, and the distance between feeding patch and top resonators is 1.4 μm.

B. Simulation and Optimization

The proposed antenna was simulated and designed using full 3-D electromagnetic (EM) structure simulator (Ansoft HFSS). The simulation results of the proposed antenna according to the design variables are shown in Fig. 2. As shown in Fig. 2 (a), the resonant frequency decreases as the size of top resonator (W_{SR}) increases. The effects of the feeding patch size (W_F) and spacing between stacked resonators (G_{SR}) on the return loss are plotted in Fig. 2 (b) and (c), respectively. When W_F is 155 μm and G_{SR} is 5 μm, the maximum bandwidth of return loss can be achieved. From these simulation results, the optimum dimensions are determined as follows: W_{SR} = 230 μm, L_{SR} = 240 μm, W_F = L_F = 155 μm.

Fig. 3 shows the comparison of return loss and radiation efficiency between the proposed antenna and the standard rectangular patch antenna. The radiation efficiency and fractional bandwidth of 10-dB return loss of the proposed antenna are 18.7% and 12.3%, while those of the standard rectangular patch are 11.3% and 4%, respectively.

III. Fabrication and Measurement Results

The designed antenna has been fabricated using a 65-nm CMOS technology. Fig. 4 (a) shows the photograph of the fabricated antenna. The return loss was measured at *H*-band by on-wafer probing. The radiation characteristics such as beam pattern and antenna gain were measured using the measurement setup shown in Fig. 4 (b). The output signal of WR-03 power source is injected into the antenna through WR-03 waveguide and GSG RF probe. Then, the radiated power of the designed antenna is received by a zero-bias detector with WR-03 standard horn antenna. The horn antenna can be moved along the semi-circular arm to measure the radiation pattern and 3-dB beam width of the antenna in the E- and H-planes. The gain of the antenna is measured based on gain comparison method. The efficiency of the antenna, then, is calculated the measured gain and 3-dB beam width.

Fig. 5 shows the measured return loss of the designed antenna which is greater than 9.5 dB from 256 to 328 GHz, which corresponds to the fractional bandwidth of 24%. The maximum radiation efficiency of 16.9% was measured at 295 GHz. The resonant frequency difference between simulation and measurement seems to be caused by the parasitic capacitance of RF pad and dummy metals.

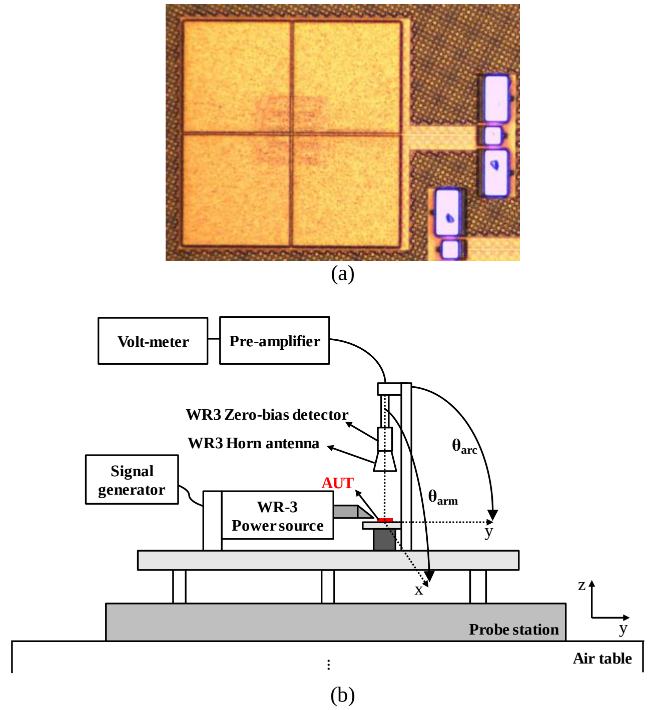

Fig. 4. (a) Fabricated on-chip antenna and (b) antenna measurement setup.

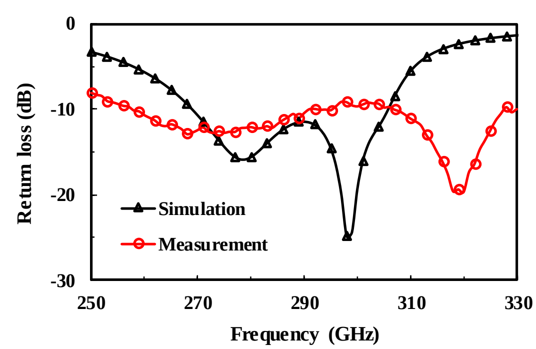

Fig. 5. Measured and simulated return loss of fabricated on-chip antenna

IV. Conclusion

In this paper, we proposed a broadband and high efficiency THz CMOS on-chip antenna. The proposed on-chip antenna employed four rectangular resonators on top of the microstrip patch antenna. It was designed and fabricated using 65-nm CMOS technology. Its simulation and measurement results showed a fractional bandwidth for 10-dB return loss greater than 10% and a radiation efficiency greater than 15.0% at 300 GHz.

Acknowledgment

This research was supported by a grant to Terahertz Electronic Device Research Laboratory funded by Defense

Acquisition Program Administration, and by Agency for Defense Development (UD150043RD).

References

[1] T. Tajima, H.-J. Song, and M. Yaita, “Compact THz LTCC receiver module for 300-GHz wireless communications,” IEEE Microw. Wireless Compon. Lett., vol. 26, no. 4, pp. 261–293, Apr. 2016.

[2] T. Bryllert, V. Drakinskiy, K. B. Cooper, and J. Stake, “Integrated 200–240-GHz FMCW radar transceiver module,” IEEE Trans. Microw. Theory Techn., vol. 61, no. 10, pp. 3808–3815, Oct. 2013.

[3] R. Han, Y. Zhang, D. Coquillat, H. Videlier, W. Knap, E. Brown, and K. K. O, “A 280-GHz Schottky diode detector in 130-nm digital CMOS,” IEEE J. Solid-State Circuits, vol. 46, no. 11, pp. 2602 - 2612, Nov. 2011.