Bandwidth and Efficiency Enhancement of Terahertz CMOS Patch Antenna

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Abstract

This paper discusses the bandwidth and efficiency enhancement of an on-chip patch antenna in 65-nm CMOS technology. V-shaped patch with slots is selected as a basic THz antenna. An additional patch is stacked on top of it to generate multiple resonances for wide bandwidth. Radiation efficiency is improved by placing slots on the ground plane. The proposed patch antenna achieves the bandwidth of 10-dB return loss of 15.5% and a radiation efficiency of 16.0% at 300 GHz with smaller chip area compared with the standard patch antenna.

Keywords: On-chip patch antenna, terahertz antenna, CMOS antenna, stacked resonator.

1. Introduction

On-chip antennas are not only easy to manufacture and integrate with active circuits because they do not require off-chip connection and packaging, but also they can achieve an excellent system performance due to the reduced parasitic effect and losses [1]. In general, on-chip antennas in nanometer-scale CMOS process utilize the dielectric between metal layers as a substrate, which can minimize the effect of lossy Si substrate. Therefore, they exhibit the poor performance in terms of bandwidth and radiation efficiency typically less than 10%, which is caused by very thin thickness of the dielectric substrate and increased conductor loss [2]. In this paper, an on-chip patch antenna with wide bandwidth and high radiation efficiency is proposed using slotted V-shaped patch and stacked resonator.

2. Antenna design

In this work, V-shaped patch is selected as a basic antenna because it can have a reduced chip area compared with the standard rectangular. Fig. 1 shows the proposed antenna with V-shaped patch. The slots are formed in the patch, which can create multiple resonances. The resonator, which is stacked on top of the patch, is designed to have different resonance frequency from that of the patch. In addition, the

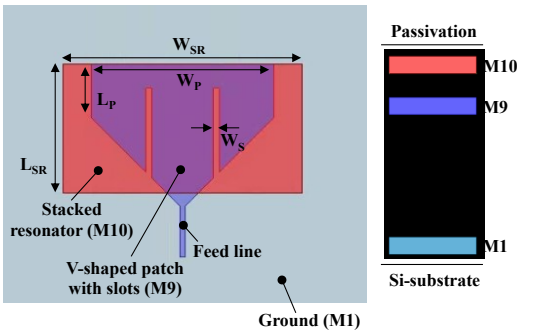

Fig 1. V-shaped patch antenna with stacked resonator using 65-nm CMOS process

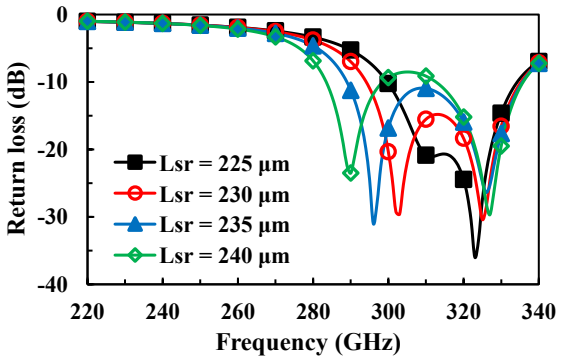

Fig 2. The simulated reflection coefficients of the proposed patch antenna with various lengths of stacked resonator (L_{SR})

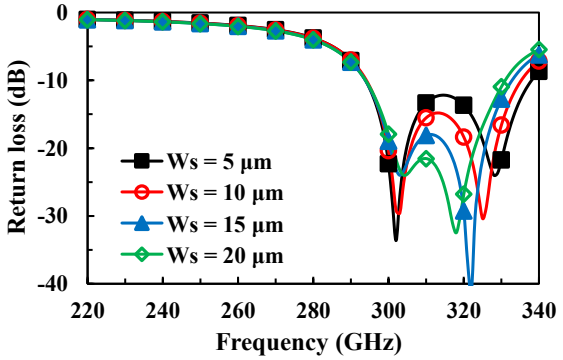

Fig 3. The simulated reflection coefficients of the proposed patch antenna with various widths of slot (W_S)

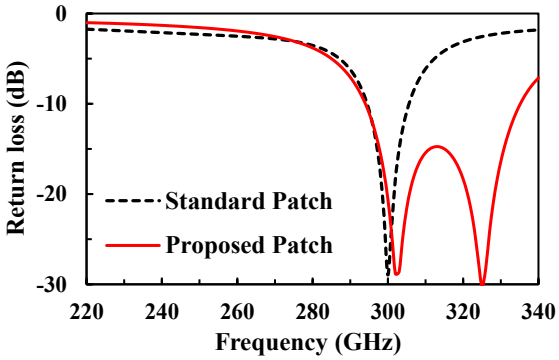

Fig 4. The simulated reflection coefficients of the standard patch and the proposed patch.

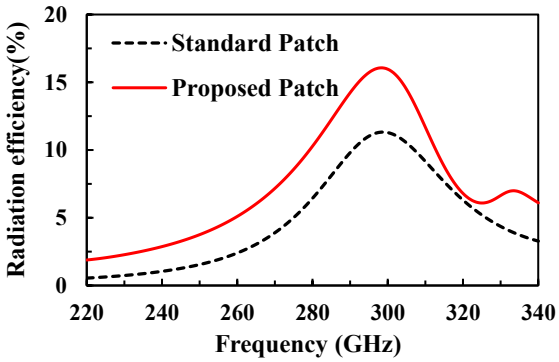

Fig 5. The simulated radiation efficiencies of the standard patch and the proposed patch.

Bandwidth can be improved by the coupling effect between the patch and the resonator [3].

The proposed antenna has been fabricated using 65-nm CMOS technology with total ten metal layers. The proposed antenna is simulated using full 3-D electromagnetic (EM) structure simulator (Ansoft HFSS). EM model is shown in Fig. 1. The slotted V-shaped patch is designed on the metal layer of M9. Uppermost metal layer M10 is used as the resonator, and lowermost metal layer M1 as a ground plane. Fig. 2 shows the simulated input return loss depending on the length of the stacked resonator (L_{SR}) which can vary the resonance frequency. The width of the slots in the patch (W_S) can also affect the resonance frequency as shown in Fig. 3. From these simulation results, the optimized dimensions are determined as follows: L_{SR} = 230 μm, W_S = 10 μm, W_{SR} = 425 μm, W_P = 325 μm, and L_P = 95 μm.

Fig. 4 and Fig. 5 shows the comparison of reflection coefficient and radiation efficiency between the proposed antenna and the standard rectangular patch. The size of the standard rectangular patch is 350 × 225 μm^2. The proposed patch antenna enhances the bandwidth of 10-dB return loss by 11.8% and radiation efficiency by 13.8% at 300 GHz. The directivity and gain of the proposed patch antenna are -0.1 dBi and 7.6 dB, respectively, at 300 GHz.

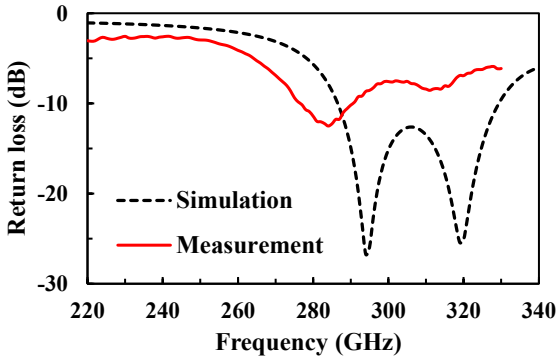

Fig 6. The simulated and measured reflection coefficient of the proposed patch.

3. Measurement and discussion

Fig. 6 shows the measured return loss of proposed patch antenna together with the simulation result. S-parameter of the fabricated antenna was measured on-wafer probing from 220 to 325 GHz. The measured return loss is better than -10 dB from 275 to 292 GHz, which corresponds to the fractional bandwidth of 6.3%. The resonant frequency was decreased by 15 GHz compared with the simulation, which is caused by the parasitic capacitances of RF pad, dummy metals, and etc.

4. Conclusion

In this paper, an on-chip patch antenna for wide bandwidth and high radiation efficiency is suggested. Simulation results shows high reflection coefficient 10-dB bandwidth of 15.5% and high radiation efficiency of 16.0% at 300 GHz.

Acknowledgement

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